Method of Forming a Polycrystalline Silicon Layer

Cross Reference

This application claims the benefit of Korean Patent Application No. 1999-67846, filed on December 31, 1999, under 35 U.S.C. § 119, the entirety of which is hereby incorporated by reference.

Background of the invention

Field of the invention

The present invention relates to a method of forming a polycrystalline silicon layer of a switching element, for example, a thin film transistor (TFT).

Description of Related Art

A thin film transistor (TFT) includes an insulating layer, a passivation film, electrode layers and a semiconductor layer. The insulating layer is made of SiNx, SiO_2, Al_2O_3 or TaOx. The passivation film is made of a transparent organic insulating material or a transparent inorganic insulating material. The electrode layer includes a gate electrode, a source electrode and a drain electrode and is made of a conductive metal such as Al, Cr or Mo. The semiconductor layer acts as a channel region along which charges flow and is made of amorphous silicon or polycrystalline silicon.

A process of forming the semiconductor layer using the amorphous silicon can be performed at a low temperature of about 350 °C and thus is relatively simple. However, since a field effect mobility of the amorphous silicon layer is as low as 2 $cm^2/V•sec$, thus, switching characteristics of the TFT and an incorporation characteristics between a driving circuit and the TFT are not so good.

Meanwhile, the polycrystalline silicon layer is much more excellent in response speed than the amorphous silicon layer. The polycrystalline silicon layer has as a high field effect mobility as about 20 $cm^2/V•sec$ to about 550 $cm^2/V•sec$. A switching

speed of the TFT depends on the field effect mobility. That is, a switching speed of the polycrystalline silicon layer is 100 times as fast as that of the amorphous silicon layer. This comes from that the polycrystalline silicon layer is more in grain number and is smaller in defect than the amorphous silicon layer.

A method of forming the polycrystalline silicon layer includes an eximer laser annealing technique, a solid phase crystallization (SPC) technique, and a metal induced crystallization (MIC) technique.

The eximer laser annealing technique is performed at a low temperature and, thus a low-cost glass substrate is used. The TFT manufactured using the eximer laser annealing technique has a field effect mobility more than 100 $cm^2/V \cdot sec$ and thus is excellent in operating characteristics.

The solid phase crystallization technique is one which amorphous silicon is crystallized at a high temperature of more than 600 °C. Since a crystallization is performed at a solid phase, a grain has many defects such as a micro-twin, a dislocation and the like, whereupon a grade of a grain is low. In order to compensate for this problem, a thermal oxidation film of about 1000 °C is used as a gate insulating layer. Therefore, since a high-cost material such as quartz is used for the substrate, there is a problem that a production cost is high.

The metal induced crystallization technique is one that a crystallization is performed in such a way that a metal layer is deposited on the amorphous silicon layer and then a heat treatment is performed. The metal layer serves to lower an enthalpy of the amorphous silicon layer. As a result, a process is possible at a low temperature of about 500 °C. However, a surface state and electrical characteristics are not so good. This technique also causes many defects in grain.

The polycrystalline silicon layer manufactured using the techniques described above can obtain grains from silicon seeds while the silicon of a liquid state is cooled at the beginning stage of crystallization. In case that a grain of the silicon grows laterally, large-sized grains can be obtained. If a distance between adjacent silicon seeds is greater than a maximum silicon growth distance, the silicon grain that performs a lateral growth centering the silicon seed grows maximally, and then a small-sized grains are created on a region of a liquid state due to a nucleus generated by a super-cooling. However, a distance between adjacent silicon seeds is smaller than a maximum silicon growth distance, a lateral growth occurs centering a seed, forming grain boundaries, whereby the polycrystalline silicon layer having large-sized grains is formed. As described above, in order to obtain the excellent TFT, the large-sized grains should uniformly be arranged while forming the grain boundaries.

Figs. 1A to 1C are plan views illustrating a crystallization process of a polycrystalline silicon layer. A distance between the two adjacent silicon seeds 11 is smaller than a maximum grain growth distance, but it is desirable that the silicon seeds 11 are uniformly distributed. The silicon grains 13 of a liquid state grow laterally centering on the silicon seed 11 and complete their growth while forming grain boundaries 15.

Hereinafter, a crystallization process of the polycrystalline silicon layer using the eximer laser annealing technique according to a conventional art is explained in detail.

Fig. 2 is a perspective view illustrating a configuration of a polycrystalline silicon crystallization equipment using the eximer laser annealing technique. The equipment includes a laser beam device (not shown), a mask 33, and a projection lens

35. The projection lens 35 is arranged over a substrate 31, and the mask 33 is aliened with the projection lens 35. When a laser beam 37 is projected from the laser beam device toward the mask 33, the laser beam 37 becomes incident along the mask pattern. The laser beam incident to the mask 33 passes through the projection lens 35 and is concentrated on a substrate 31 having an amorphous silicon layer formed thereon, whereby polycrystallization of the amorphous silicon layer is performed according to the mask pattern.

At this point, a growth of the polycrystalline grain is controlled by a shape and an energy density of the laser beam and a temperature and a cooling speed of the substrate. A silicon grain during a crystallization process is divided into three regions: a low energy density region; an intermediate energy density region; and a high energy density region. The low energy density region is a partially melt region. That is, the lower energy density region is one which only a lower portion of the silicon layer is not melt and a silicon melting depth is smaller than a thickness of the silicon layer and a grain diameter is smaller than a thickness of the silicon layer because seeds on the lower portion of the silicon layer grow vertically.

The intermediate energy density region is an almost completely melt region. That is, the intermediate energy density is one which only part of seeds on the lower portion of the silicon layer is not completely melted. Except for part of seed on the lower portion of the silicon layer, almost part of the silicon layer is completely melted. This region is also a region that a lateral growth is possible centering on the seeds.

The high energy density region is one that even the lower portion of the silicon layer is completely melted.

A crystallization method using the polycrystalline silicon crystallization

equipment of Fig. 2 is as follows. The laser beam 37 is uniformed by predetermined means. Thereafter, a type of a laser beam that will be formed on the substrate 31 is determined through the mask 33. A laser beam having a width of tens of is formed through the projection lens 35. The substrate 31 arranged on a stage moves slowly at a speed of less than 1 /pulse, so that a crystallization is performed by the laser beam. The mask 33 has divided regions "A", "B", and "C" in shape of stripe.

Fig. 3 is a plan view illustrating a mechanism that the amorphous silicon layer is crystallized through the laser beam. At this time, in first and second crystallization steps 45, a lateral growth occurs by moving the substrate 31. At the second step, a grain boundary 41 of the first step moves and forms a new grain boundary 41a.Preferably, a high energy density for complete melting is used, and a width of the laser beam is smaller than twice of the maximum lateral growth distance.

After an n-th crystallization step, grains of the polycrystalline silicon that is crystallized by the lateral growth grows as large as a grain 43 and the grain boundary 41n is finally determined.

Fig. 4 is an enlarged view illustrating a portion D of Fig. 3. As shown in Fig. 4, the polycrystalline silicon layer has a protruding portion 45 that protrudes upwardly due to a later growth of the adjacent grains and is formed on the grain boundary. This is because the solid silicon is greater in volume than the liquid silicon, and the silicon layer melted is lastly cooled at the grain boundary region, increasing a volume. The protruding portion 45 has a height of about 300 Å.

Further, when the silicon layer is crystallized using the conventional crystallization described above, as shown in Fig. 5, defects 51, referred to as a low angle defect, may exist on the surface of the layer. This is because the heat energy contained

in the silicon layer is suddenly exhausted via the substrate below the silicon layer when the laser beam is blocked.

The defects on the surface of the silicon layer result from the sudden cooling, leading to an abnormal growth of the grains.

The polycrystalline silicon layer manufactured by the above-described method is patterned for a channel of the semiconductor layer in subsequent process, and then an insulating layer is formed on the polycrystalline silicon layer. In other words, since the insulating layer is formed on a non-flat surface of the semiconductor layer due to defects in the gains and the grain boundary protruded upwardly, a trap level may occur due to a mismatch between the polycrystalline silicon layer and the insulating layer. Therefore, field effect mobility of charges that flow along a surface of the polycrystalline silicon layer is significantly lowered, leading to a low reliability.

SUMMARY OF THE INVENTION

To overcome the problems described above, preferred embodiments of the present invention provide a method of forming a polycrystalline silicon layer having excellent electrical characteristics.

In order to achieve the above object, the preferred embodiments of the present invention provide a method of forming a polycrystalline silicon layer, comprising: forming an amorphous silicon layer on a substrate; a first step of melting completely the amorphous silicon layer using a laser beam thereby forming the polycrystalline silicon layer by adopting a mask; and a second step of melting an upper portion the polycrystalline silicon layer using the laser beam by adopting the mask thereby recrystallizing the upper portion of the polycrystalline silicon layer.

The mask has a completely melting region and a partially melting region. The completely melting region and the partially melting region have stripe shapes. The completely melting region and the partially melting region are postioned in series. The completely melting region of the mask pattern is made of a material having a high light transmittance, and the partially melting region of the mask pattern is made of a material having a low light transmittance. The first and second steps are proceeded through one scanning process of moving the substrate having the amorphous silicon layer under the laser beam.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

Figs. 1A to 1C are plan views illustrating a typical crystallization process of a polycrystalline silicon layer;

Fig. 2 is a schematic perspective view illustrating a configuration of a polycrystalline silicon crystallization equipment using the eximer laser annealing technique;

Fig. 3 is a plan view illustrating a mechanism that an amorphous silicon layer is crystallized through the polycrystalline silicon crystallization equipment of Fig. 2;

Fig. 4 is an enlarged side view of "D" portion of Fig. 3;

Fig. 5 is a detailed plan view illustrating a surface of a polycrystalline silicon layer formed according to a conventional method;

Fig. 6 is a plan view illustrating a mask pattern for the laser beam according to an embodiment of the invention;

Fig. 7 is a plan view illustrating a crystallization process according to the embodiment of the invention; and

Fig. 8 is a cross-sectional view illustrating a polycrystalline silicon layer formed by a method of the embodiment of the invention compared to that formed by a conventional method.

DETAILED DESCRIPTION OF PREFFERED EMBODIMENTS

Reference will now be made in detail to a preferred embodiment of the present invention, example of which is illustrated in the accompanying drawings.

The forming method for a thin film transistor is follows. First, a gate electrode and a gate line (not shown) are formed on a substrate (not shown). Thereafter, an insulating layer of SiNx or SiO_2 is formed over the whole surface of the substrate. An amorphous silicon layer is deposited on the insulating layer. In case that the amorphous silicon layer is made of hydrogenized amorphous silicon, a dehydrogenation process is performed to remove hydrogen in advance before a crystallization process. It is because pores, which may lower electrical characteristics of the polycrystalline silicon layer, may be formed while hydrogen is removed during the crystallization process.

Sequentially, the amorphous silicon layer is crystallized using the mask pattern 109 shown in Fig. 6 and undertakes a lateral growth to form the polycrystalline silicon layer. At this point, the mask pattern 109 includes a partially melting region 111 and a completely melting region 113 in series. On the partially melting region 111, a coating film having a low light transmittance is formed, while the completely melting region

113 has a good light transmittance. Therefore, the laser beams that pass through the partially melting region 111 and the completely melting region 113 become different in energy intensity. The partially melting region 111 is a region that corresponds to the low density energy region which melts the silicon layer less than its full depth, whereupon only an upper portion of the polycrystalline silicon layer can be melted. On the other hands, the completely melting region 113 is a region that corresponds to the high energy density region. The laser beam that passes through the completely melting region 113 has a width of about 2 and completely melts the amorphous silicon layer, so that a later growth can be sequentially performed. The completely melting region 113 and the partially melting region 111 have a stripe shape. The completely melting region 113 advances the partially melting region with respect to the scanning direction.

Hereinafter, a method of forming the polycrystalline silicon layer having a flat surface according to the preferred embodiment of the present invention is explained with reference to Fig. 7. As shown in Fig. 7, during a first laser annealing process, the laser beam scans the amorphous silicon layer deposited on the substrate 211 using the mask pattern 109. Portions 113a, 113b and 113c of the silicon layer are completely melted by the laser beam via the completely melting region 113, and other portions 111a, 111b and 111c of the silicon layer are partially melted by the laser beam via the partially melting region 111 of the mask pattern 109 (Fig. 6).

Subsequently, by moving the substrate 211, the polycrystalline silicon layer that is formed by the completely melting region 113 of the mask pattern 109 is scanned by the laser beam that passes through the partially melting region 113 of the mask pattern 109, so that upper portions of the firstly completely melted portions 113a, 113b and 113c of the polycrystalline silicon layer is recyrstallized up to a predetermined

depth. Therefore, the polycrystalline silicon layer having grains of no defect and a flat surface can be manufactured. By moving the substrate sequentially, the complete melted portions 113a, 113b and 113c are fully recrystallized by the laser beam via the partially melting region 111 of the mask pattern 109. That is, the partial melting is sequentially performed at the same time, and the crystallization process is completed at an nth laser annealing process. The scanning process is completed when all the completely melted portions are over scanned by the laser beam via the partially melting region of the mask pattern 109.

Fig. 8 is a cross-sectional view illustrating a portion of the polycrystalline silicon layer according to the preferred embodiment of the present invention. As shown in Fig. 8, the polycrystalline silicon layer formed through the first laser annealing process has a protruding portion "F" formed on the grain boundary region that the adjacent grain boundaries contact with each other. The protruding portion "F" is melted and recrystallized through the second laser annealing process, so that the polycrystalline silicon layer becomes flatted. Then, using the method described above, the polycrystalline silicon layer having a flat surface is patterned into the semiconductor layer in the form of an island. Then, source and drain electrodes (not shown) spaced apart from each other are formed to overlap both end portions of the semiconductor layer. Therefore, the switching element according to the preferred embodiment is completely manufactured. In the preferred embodiment of the present invention, an inverted staggered TFT is exemplary explained, but the polycrystalline silicon layer can be employed in a top gate type TFT.

As described herein before, using the method of forming the polycrystalline silicon layer according to the preferred embodiment of the present invention, defects in

the grains can be removed, and also the protruding portion formed on the grain boundary region becomes flatted. Therefore, the switching element having excellent electrical characteristics can be obtained.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.